Call for Papers

DFT 2002 will be held in Vancouver, Canada, a colorful and charming site for this seventeenth issue in a series of interesting and productive technical meetings, favouring fruitful exchanges between academic and industrial attendees.

The symposium will provide an open forum for presentations in the field of defect and fault tolerance in VLSI systems. One of the unique features of this symposium has been, and will be, to combine new academic research to state of the art industrial data, necessary ingredients for significant advances in this field. All aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation are of interest. We are inviting new and unpublished papers on, but not limited to, the following topics:

1. **Yield Analysis and Modeling**
   - defect/fault analysis and models; statistical yield modeling; critical area and other metrics; on-line data collection; product planning

2. **Yield Enhancement**
   - IC layout modification for manufacturability; process control and measurement

3. **Repair, Restructuring and Reconfiguration**
   - mechanism for fault-isolation, reconfiguration, and repair; restructurable and reconfigurable circuit design; on-line reconfiguration and repair

4. **Testing Techniques**
   - built-in self-test in VLSI/WSI; built-in current sensors (BICS)/Iddq testing; delay fault model and diagnosis; parametric testing; testing for FPGA; testing for analog or mixed circuits

5. **Error Detection, Correction, and Recovery**
   - self-testing and self-checking design; error-control coding; fault masking logic design; recovery scheme by space/time redundancy

6. **Defect and Fault Tolerance**
   - cost-performance analysis of defect and fault tolerance; reliable circuit synthesis; radiation hardened/tolerant processes and design techniques; delay defect/fault tolerance

7. **Dependability Analysis and Validation**
   - fault detection techniques and environments; dependability characterization of integrated circuits and systems

8. **Case Studies and Applications**
   - giant integration by MCM/WSI; design for defect and fault tolerance in specific circuits; design for fault tolerance in processors, memories, networks, signal processing systems, FPGA-based systems and embedded systems; fault tolerance in automotive, railway, avionics, industrial control, and space applications

A Special Session on Wafer Scale/Large Area Systems (>5 cm) will also be organized, dedicated to the special requirements of devices whose silicon area exceeds that of a single reticle print and yet are implemented on a single substrate.

Prospective authors should prepare an extended summary or the full paper (up to 9 pages in the IEEE 6X9 format), to be submitted as PDF file. Uncompressed unencapsulated postscript may also be used when necessary. Submission will be electronically only. Use the contact author's last name as file name; add numerals in the case of multiple submissions (e.g., lo1, lo2). Detailed information about the submission process will be made available on the symposium Web page:

http://www.elet.polimi.it/dft/

Authors should notify their submission to both the Program co-Chairs by email, indicating the title, authors name, affiliation, mail address, phone, fax and e-mail and the name of the contact author. The submission should also indicate the intended presenter. We are also interested in panel sessions that involve industrial experiences: please send an email to the Program Chairs with a brief description of the panel discussion you would like to propose.

Prospective authors should adhere to the following deadlines:

- **extended summary due date:** May 30, 2002
- **notification of acceptance:** July 1, 2002
- **camera ready full papers:** August 10, 2002

The proceedings will be published by the IEEE Computer Society. Authors will have the opportunity to submit extended versions of the papers published at the symposium for planned special section in the IEEE Transactions and Journal of System Architecture.

For general information, contact the General co-Chairs. For paper submission information, contact one of the Program co-Chairs. For all updated information concerning the symposium, visit our Web page.