NoCTrace - A System Level Architecture Exploration Tool for Network on Chip Architectures

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Abstract:

Besides the programmability also the efficiency of many-core architectures needs to be considered with respect to the employed parallel programming models. The execution of parallel programming models is often very demanding in terms of processing power and data transfers. In order to find an appropriate and efficient implementation e.g. on NoCs, it is very important to be able to adapt the system to the programming model at design time. Additionally the different alternatives need to be explored in their implementation efficiency on the various system setups. The needed profiling/exploration methodology differs strongly from well known techniques for e.g. scalar processor architectures, due to the fact that the profiler has to reflect the different configurations of the computing platform.

The poster presentation addresses methodologies to profile/explore configurable parallel computing platforms in respect to their accompanied parallel programming models.

In detail we present our implementation of a specialized system level architecture exploration tool called NoCTrace, which uses SystemC as input for the architectural description of the parallel computing system. Without using instrumentation techniques our tool provides the user with a deep analysis of the system.

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Motivation
Find a generic, non intrusive system level exploration methodology for SystemC architecture models

- Extract profiling data from system platform simulation model runs
- Non intrusive data collection
  - No need to instrument simulated software model
  - No need to instrument platform simulation model

Basic Concept
- Extract/record program counter and transaction data in SystemC kernel
- Automatic design analysis enables easy tool adaption to the current platform model

Tool Architecture
- NoCTrace backend
  - Collects data
- NoCTrace frontend
  - Processes data
  - Manages data (persistency)
  - Presents data (GUI)

Tool Workflow
- Compile platform simulation model with SystemC library including NoCTrace stubs
- Start simulation
- After elaboration phase the simulation breaks
- Verify proposed transaction monitors and identify program counter name
- Continue simulation
- Configuration for simulation model will be persistently stored
- Repeated automated simulation runs easily possible

Use Cases
- Analyze SystemC architectures
- Generate network load figures of NoCs
- Analyze network traffic in NoCs
- Optimize memory access in NoCs
- Optimize runtime systems
- Optimize parallel programming models

Profile Example