Heterogeneous multi-processor systems (HMPS) have been recently exploited for a wide range of application domains, for both the general-purpose and the dedicated products. Such systems include several processors, memories, and a set of interconnections between them. Moreover, by definition, the set of processors in the same architecture is heterogeneous. This implies that it is possible to have, at the same time, one or more items of the following:

- COTS (i.e. Common-Off-The-Shelf) general-purpose processors (e.g. x86, ARM, etc…)
- COTS domain-oriented processors (e.g. Digital Signal Processor, Network Processor, etc…)
- Custom domain-oriented processors (the so called Application Specific Instruction Processors)
- COTS single-purpose processors (e.g. AES encoder/decoder, JPEG encoder/decoder, etc…)
- Custom single-purpose processor (i.e. the actual ad-hoc developed HW component)

In the scope of this work, a dedicated system is a digital (sometimes mixed) electronic system with an HW/SW custom architecture designed in order to satisfy specific a priori known application requirements (functional and non-functional). A dedicated system could be embedded in a more complex system or it could be subjected to real-time constraints. Often, both the previous situations could apply.

When dedicated systems are also HMPS, one consideration is always true: they are so complex that the design methodology plays a major role in determining the success of the products.

In fact, in the past years, a remarkable number of research works have focused on system-level co-design of HMPS. Each of them has proposed a (quite) different approach to the design space exploration but all of them always rely on a (quite) fixed target architecture or (quite) heavily rely on the designer experience to define some of the target architecture features. In particular, the definition of the communication architecture (i.e. the interconnection links details and the topology) is always only a input to the design flow (typically imposed by a platform-based approach). So, at the best of our knowledge, it doesn’t exists a system-level design flow that addresses the problem of automatically suggest an HW/SW partitioning of the application specification also mapping the partitioned entities onto an automatically selected dedicated heterogeneous multiprocessor architecture (being aware of both computation and communication components).

According with this scenario, this work faces the problem of the HW/SW co-design of dedicated systems based on heterogeneous multi-processor architectures. In particular, it proposes a system-level design space exploration approach able to automatically suggest to the designer:

- an HW/SW partitioning of the application;
- a dedicated HMPS architecture;
- a mapping of the partitioned entities onto the proposed architecture.

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Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications

System-Level Design Space Exploration for Dedicated Heterogeneous Multi-Processor Systems

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Overview

Such extensions allow the methodology to propose an HW/SW partitioning of the specification, mapping the partitioned entities onto an automatically selected heterogeneous architecture, being aware of both the computational and communication components

Architectural Elements & Metrics

Saturation Index

Exploitation Index

Total Cost

Cost Function

Example: Step 1

Annotated Specification (CSP)

Example: Step 2

Executors/Allocation View

Example: Step3

Executors Interaction Graph

Example: Step 4

Results

Example: Step 4 bis

Results