Optimization of an Embedded Parallel System-on-Chip Platform using modeFRONTIER

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Abstract

A complete design space analysis of a System-on-Chip (SoC) architecture is prohibitive due to the huge number of architectural configurations and long simulation time.

A statistical test can reduce the search space which can be exhaustively explored. An alternative choice is to rely on an optimization algorithm which does not lose degrees of freedom and it focuses the efforts towards the set of optimal trade-off designs.

Both tasks require a design environment providing the ability to express the problem in clear terms during the process definition, the optimization run and the post-processing results analysis. modeFRONTIER environment offers specific tools to help designers in carrying on these activities. In the FP7-MULTICUBE project, modeFRONTIER has been retargeted to SoC design domain in terms of interaction with SoC simulators and introducing ad hoc algorithms for discrete and categorical problems.

We tested a new genetic algorithm MFGA against state of the art statistical approach on a test case provided by STMicroelectronics. The analysis of the results gives a deep insight on the proposed application and it contributes to increase the confidence in the capabilities of automatic optimization of SoC platforms in terms of accuracy of the results (against the optimal solution) and exploration time.