AccurateTime-to-Digital Converter based on Xilinx's Digital Clock Managers

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Outline

- Introduction
- Improvements of our proposal
- Principles of operation
- Expected characteristics
- Experimental results
- Conclusions

Introduction

1. Time interval measurement needed (resolution < 1ns)
2. FPGA with free resources

Time to Digital Converter (TDC) implementation options

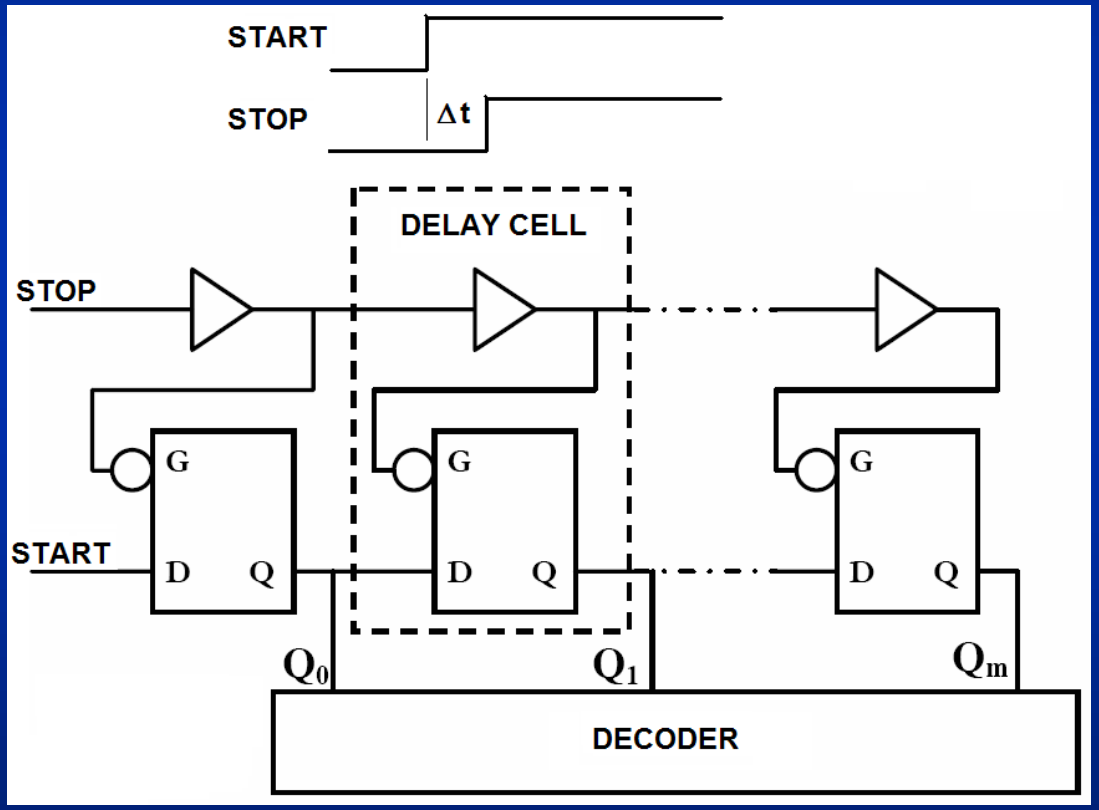
Commercial TDC

Built-in solution

Saves components, PCB (and €)

Introduction

TDC are mainly based on delay chains



τ = delay difference

Resolution = τ

$\Delta t = N\tau$

Range = $M\tau$

Introduction

Previous TDCs in FPGAs:

Implementation of delay chains using logic elements or specific resources

- 👍 Great design flexibility
- 👎 Manual placement & routing

⇩

Complex design process

- 👎 Temperature and source voltage dependence

⇩

External and recurrent calibration

Improvements of our proposal

We use the delay chains included in Digital Clock Managers (DCMs)

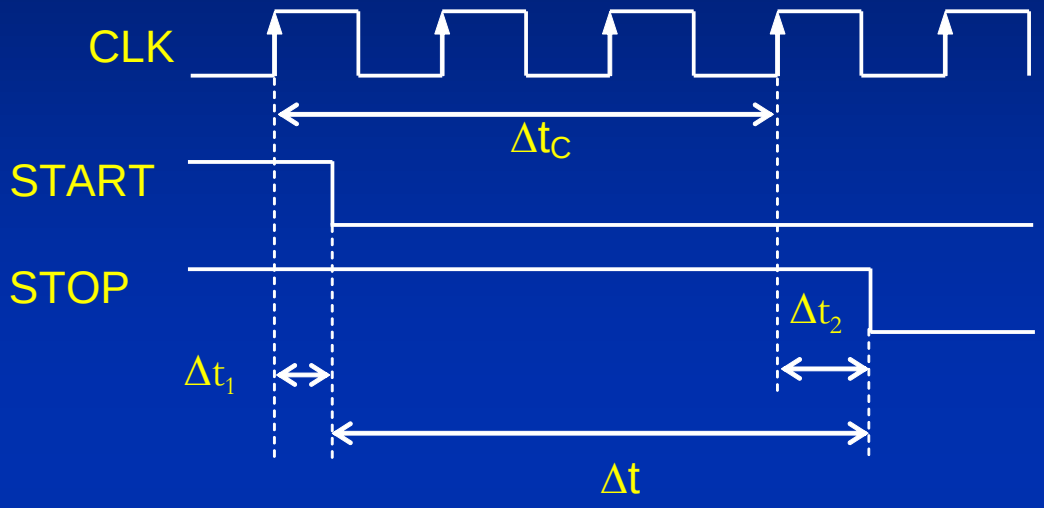
- Automatic placement & routing
- Temperature and source voltage compensated

⇩

No external calibration needed

- Lower design flexibility

Principles of operation



In general terms: $\Delta t = \Delta t_C - \Delta t_1 + \Delta t_2$

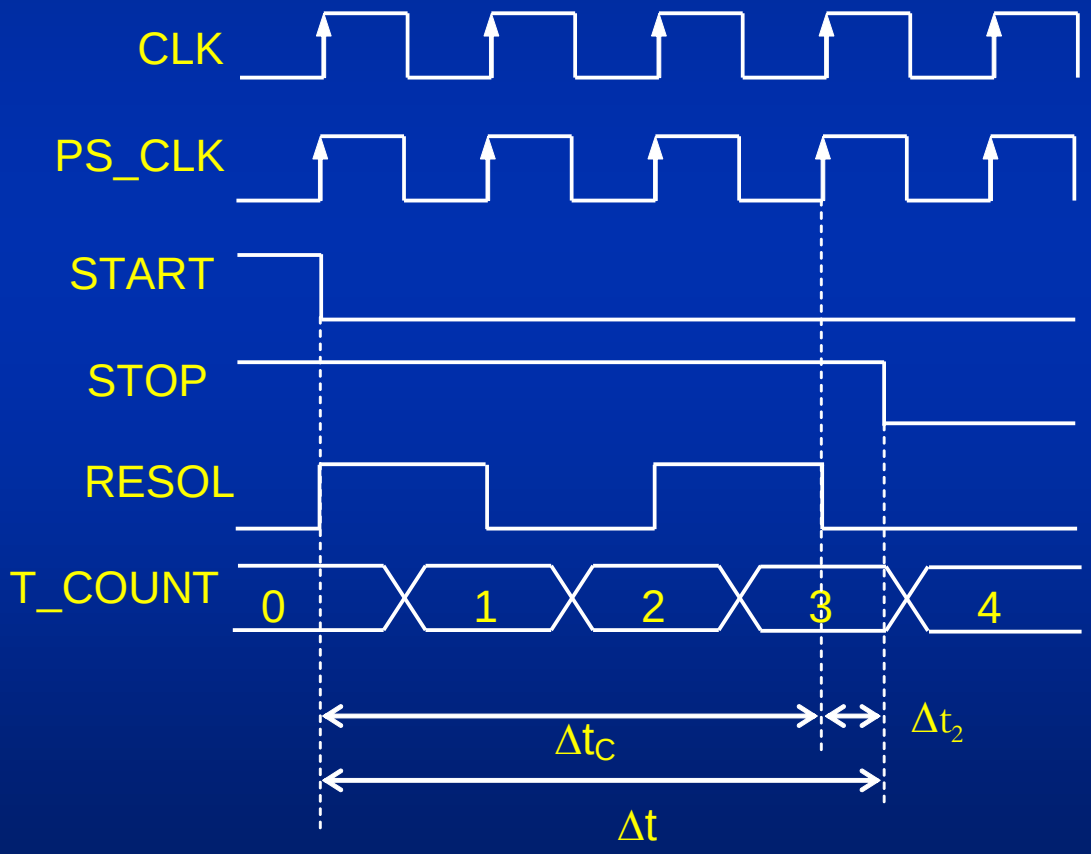
If signal START is generated from the TDC and suppousing that iternal delays are zero:

$\Delta t = \Delta t_C + \Delta t_2$

Principles of operation

Based on the phase shifting capability of DCMs

First stage: "conventional" coarse measurement

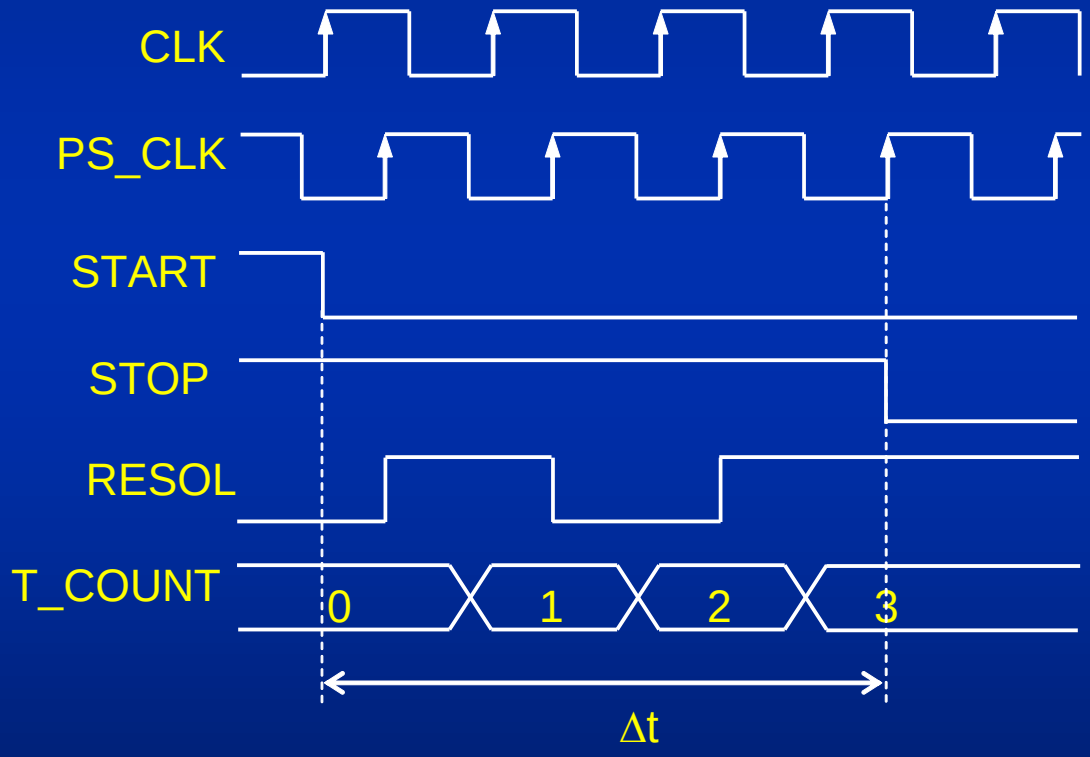


$\Delta t_C = J \cdot T_{CLK}$

Principles of operation

Based on the phase shifting capability of DCMs

Second stage: PS_CLK is shifted δt K times



$\Delta t_2 = K \cdot \delta t$

$\Delta t = J \cdot T_{CLK} + K \cdot \delta t$

Expected characteristics

- DCM configuration:

Virtex-4	
CLKOUT_PHASE_SHIFT	VARIABLE_CENTER ($\delta=T_{CLK}/256$)
DCM_PERFORMANCE_MODE	MAX_SPEED
DLL_FREQUENCY_MODE	HIGH
DESKEW_ADJUST	SOURCE_SYNCHRONOUS
Spartan-3	
CLKOUT_PHASE_SHIFT	VARIABLE ($\delta=T_{CLK}/256$)
DLL_FREQUENCY_MODE	LOW
DESKEW_ADJUST	SOURCE_SYNCHRONOUS

Expected characteristics

- Operating frequency:

  Lower than maximum

  Shifting range greater than clock period

  Frequency = 200MHz (V4), 100MHz (S3)

  Shifting step = 19.5ps (V4), 39ps (S3)

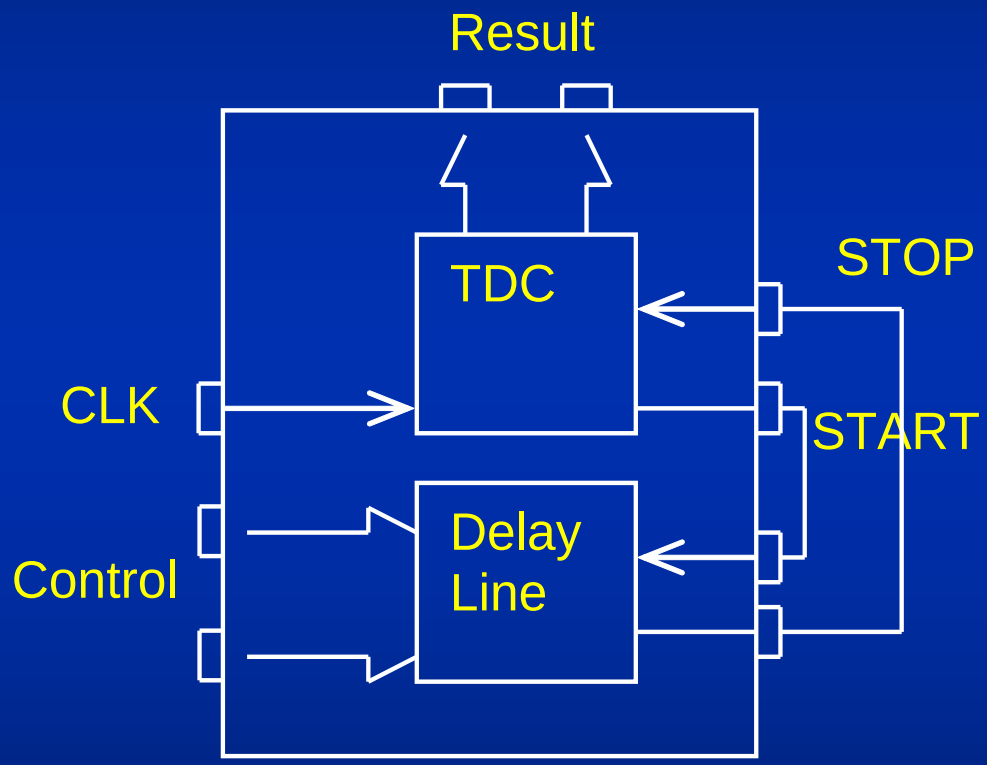
- Practical limit that increases resolution:

  Maximum period jitter: ±100ps

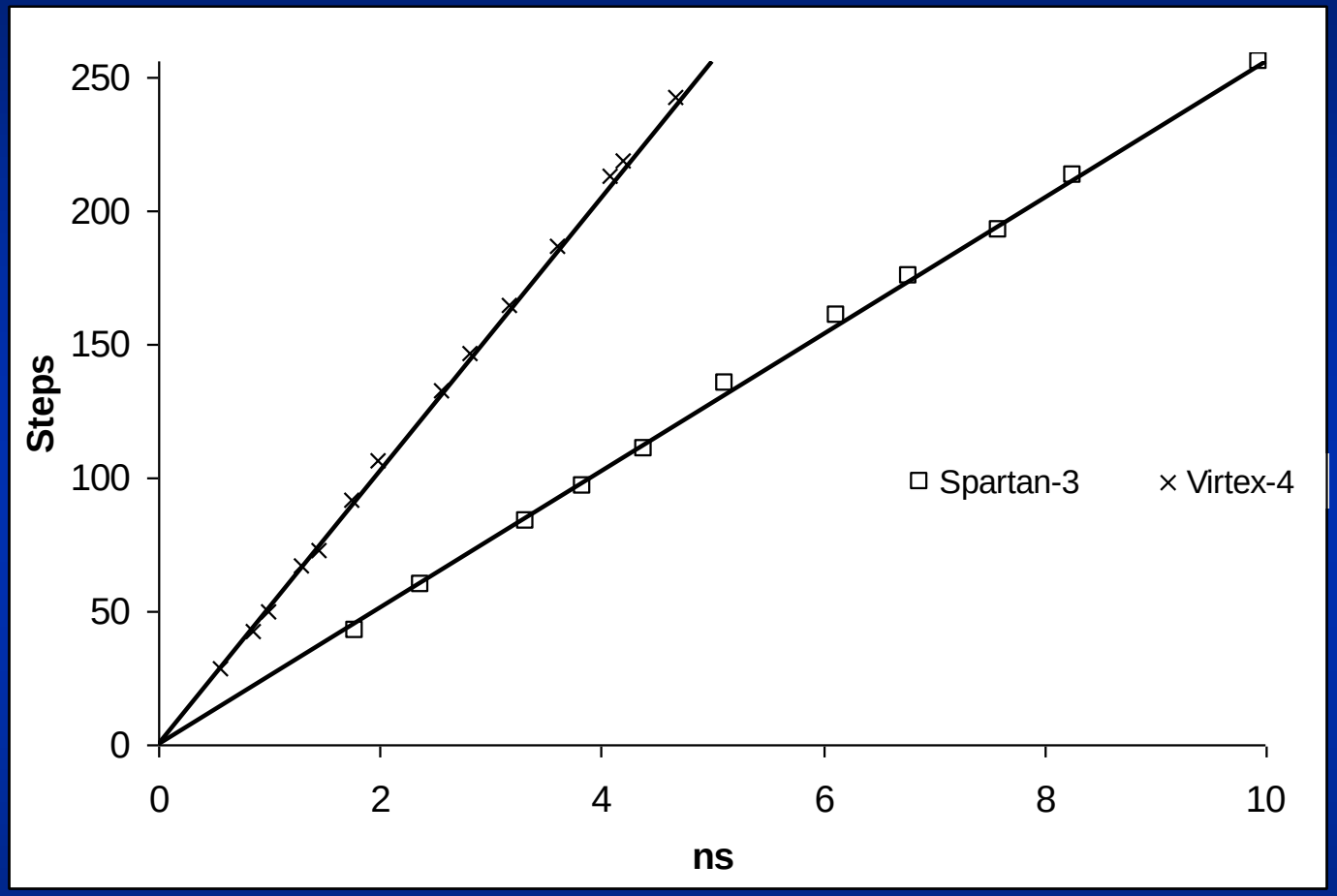
  Practical resolution: ≤ 200ps

Experimental results

Test circuit



Experimental results



Maximum difference: 111ps (V4) 169ps (S3)

Conclusions

A TDC for time measurements:

- Of static delays
- With a resolution ≤ 200ps
- With an easy implementation
- Without complex calibration

Thank You for your attention!!!