High Density Asynchronous LUT
Based on Non-Volatile MRAM Technology

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ST-Microelectronics
Outline

Introduction and motivation

- Asynchronous FPGA
- Magnetic RAM (MRAM)
- MRAM based synchronous FPGA

MRAM based Asynchronous LUT

- Operation and Configuration
- Hybrid Simulation

Conclusion
Why Asynchronous FPGA?

- Higher throughput
- Lower power
- (Smaller die area)

R. Manohar, HPEC 2009
Why Magnetic RAM (MRAM)?

Leakage issue : Configuration memory and FF !

SRAM based synchronous FPGA

Non-volatile memory is required

Conventional CMOS technology

W/O loss of data!
Why Magnetic RAM (MRAM)?

- High Write/Read Access speed
- High density and 3D integration
- Infinite endurance
- Low Write/Read power
- Radiation hardness
- ......

Storage based on the spin property of electron

Thermally Assisted Switching (TAS) Approach: 2011

Spin Transfer Torque (STT) Approach: 2012

1st Commercial MRAM product (2006)

SIEMENS 2008

AIRBUS 2009

Field induced Magnetic Switching (FIMS):

High switching power and errors!!
MRAM based Synchronous FPGA

Configurable logic block (CLB)

MRAM based synchronous FPGA

WS. ZHAO et al., FPT, 2007

WS. ZHAO et al., ACM TECS, 2009

Y. Guillemenet, et al., FPL, 2008
MRAM based Synchronous FPGA

- Zero standby power
- Dynamic Reconfiguration
- Multi-context configuration
- Instant on/off
- Radiation hardness
- ...

3D integration: high density and high access speed

High dynamic power, in particular for the Magnetic Flip-Flop

\[ P_{dynamics} = f_{clk} \times \int_0^T V_{dd} \times I_d(t) dt \]

Need to be reduced ...

WS. ZHAO et al., IEEE-ICSICT, 2006

N. SAKIMURA et al., IEEE-CICC, 2008
MRAM based Asynchronous FPGA

• Higher throughput
• Lower power
  ❖ Lower dynamic power
  ❖ Zero standby power (MRAM)
• Smaller die area or high density
  ❖ Without global clock
  ❖ Without external memory (MRAM)
• Dynamic configuration and multi-context configuration (MRAM)
• Instant on/off capability (MRAM)
• Radiation hardness (MRAM)

What’s the circuits, architectures, control protocol … ?
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Pre-Charge Sense Amplifier (PCSA) for MRAM:

- Sensing delay < 200ps
- High sensing speed
- High reliability
- Easy to realize multi-context
- Small die area
- ...
PCSA based Magnetic LUT (MLUT):

Example of 1-input MLUT

Less transistors than 6-T SRAM LUT
Asynchronous Configurable Logic Block (CLB)

PCSA MRAM circuits and Pre-Charge Principle based protocol
(Re)configuration of asynchronous MRAM LUT:

Thermally Assisted Switching (TAS) Approach

Configuration circuits

JP. Nozieres et al., US 7411817, 2006

The drivers can be shared globally
Multi-context can be easily implemented and only one selection transistor is used for one bit in each context.
Hybrid MRAM/CMOS Simulations: MALUT Configuration

CMOS 130nm (STMicro)
MRAM 120nm

M. Elbaraji et al., JAP, 2010

Whole configuration delay is about 25ns
Hybrid MRAM/CMOS Simulations: MALUT Operation

CMOS 130nm (STMicro)
MRAM 120nm

M. Elbaraji et al., JAP, 2010

Operation speed: ~1GHz

The 2-input asynchronous CLB has been configured with a bit-stream “1010”.

Prototype Development: layout examples

Hybrid design kit
CMOS 130nm (STMicro)
MRAM 120nm

Layout of a 4-input MALUT
With 8 contexts
Conclusion

**1st MRAM based Asynchronous LUT**

- Higher throughput (~1GHz)
- Lower power
- Smaller die area or high density
- Dynamic configuration and multi-context configuration
- Instant on/off capability
- Radiation hardness

**Circuits: Pre-Charge Sense Amplifier**

**Architectures: Pre-Charge Asynchronous protocol based**

**Simulations: TAS-MRAM + CMOS 130nm and 65nm**

**Prototypes: 8 contexts asynchronous LUT (130nm technology)**

Innovative routing architecture
Thank you for your attention!