Improving QoS of Multi-Layer Networks-on-Chip with Partial and Dynamic Reconfiguration of Routers
Goal: Present a Multi-Layer NoC which has low area overhead and provides QoS by using partial reconfiguration features and circuit switching networks.

Motivation: Use less logic as possible for the NoC; NoC should be mainly wires. Use the right kind of NoC switching, which depends on the data being transferred.
Circuit Switching x Packet Switching

Circuit Switching
- Reserve before use
- Waste of resources if not used
+ Deterministic
+ Need small buffer
+ Good for large data exchange

Packet Switching
+ No reserve before use
+ No waste of resources
- Unpredictable timing
- Need bigger buffers
+ Good for small data exchange
  (control packets, acknowledges, monitor information, random data request/response)
Proposed Multi-Layer NoC Architecture

1. Differences
2. Responsiveness
3. Bottleneck on CC
4. Throughput
Types of NoC Routers

- **Packet Switched Router**
  - Arbitration Routing

- **Circuit Switched Router**
  - Arbitration Routing

- **Reconfigurable Circuit Switched Router**
  - No Routing Algorithm
  - No Arbitration
  - No MUXs (router logic)
  - Small buffers
Reconfigurable Router for Xilinx FPGA
### 120 (5!) Different Fixed Routers

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architecture Chave_Fixed of Chave_Fixed is
constant route: string := "NSWLE";

-- convert character (describing direction) to integer (0-4)
function c2i (c: character) return integer is
variable i: integer;
begin
    case(c) is
        when 'E' => i := 0;
        when 'W' => i := 1;
        when 'N' => i := 2;
        when 'S' => i := 3;
        when 'L' => i := 4;
        when others => i := -1;
    end case;
    return i;
end;

begin
    -- generate connections according to the constant "route"
genenerate_connections: process(rx, data_in, ack_tx)
begin
    for i in 0 to 4 loop
        tx(c2i(route(i+1))) <= not rx(i);
        data_out(c2i(route(i+1))) <= not data_in(i);
        ack_rx(i) <= not ack_tx(c2i(route(i+1)));;
    end loop;
end process;
end Chave_Fixed;
Configuration Controller performed by computer

reconfiguration requests

Data Router (Circuit Switching)

Control Router (Packet Switching)

Reconfigurable Data Router (Circuit Switching)

Compute and Forward

RS-232 cable

JTAG cable

Data in/out

Virtex4 FX12

IP
Reconfigurable Router Floorplanning
Area Results

Reconfigurable Router Configuration:
5 in / 5 out ports, 8 bits per port
14 bus-macros (5 data_in, 5 data_out, 2 control_in, 2 control_out)
28 CLBs used, 32 CLBs reserved
256 LUTs and 256 FFs reserved (2% V4FX12)

1 Left side CLB column of Bus-Macro (EAPR)
2 Right side CLB column of Bus-Macro (EAPR)
3 Router wires and inverters (EAPR)
384 LUTs and 384 FFs reserved (3% V4FX12)
### Timing Results

<table>
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<th>Description</th>
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<tr>
<td>≈ 2s</td>
<td>IP source starts sending a packet to request a new route</td>
</tr>
<tr>
<td>2 ck</td>
<td>IP source sends header to control router</td>
</tr>
<tr>
<td>6 ck</td>
<td>Delay to pass through each control router</td>
</tr>
<tr>
<td>6 ck</td>
<td>IP target (serial core) receives the entire request route packet</td>
</tr>
<tr>
<td>≈ 2s</td>
<td>Serial core sends 1 byte requesting a specific partial bitstream by the serial interface; Software running on the PC and connected to the serial interface receives the value, search this value on a table to find the name of the requested partial bitstream and call the Impact tool from Xilinx to trigger the partial reconfiguration; The Impact tool takes 54ms to send the partial bitstream by the JTAG interface running at @6MHz; After reconfiguration a byte is sent back by the serial interface to acknowledge that reconfiguration completed successfully; Finally the byte is received on the Serial core.</td>
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<tr>
<td>2 ck</td>
<td>Serial core sends a confirmation packet to control router</td>
</tr>
<tr>
<td>6 ck</td>
<td>Delay to pass through each control router</td>
</tr>
<tr>
<td>6 ck</td>
<td>IP source receives the entire confirmation packet</td>
</tr>
<tr>
<td>1 ck</td>
<td>IP source can start sending data through the established data path</td>
</tr>
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- A multi-layer NoC was presented, where a packet switching NoC is used for control and one or more circuit switching NoCs can be used for data communication.

- Partial reconfiguration is used to establish communications in the data network layer.

- Disadvantage is the initial latency for establishing a communication path.

- Advantage 1: area saving. Data routers do not need routing algorithms, arbitration and crossbars to connect input ports to output ports.

- Advantage 2: QoS. As each data layer uses circuit switching, maximum throughput is guaranteed between source and target of communication.
- Currently 120 partial bitstreams are required for each router. If partial bitstream relocation is employed, only the 120 different combinations need to be stored.
- Implement a Configuration Controller on the FPGA, not in the PC.
- Allow self-reconfiguration by using the ICAP (Internal Configuration Access Port).
- Prototype the multi-layer NoC in a bigger FPGA and improve the case study.
Questions?

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Comparing Interconnection Infrastructures

Time required to establish a communication channel

- **Packet Switched NoC (runtime)**
- **Circuit Switched NoC (runtime)**
- **Multi-Layer NoC (runtime)**
- **Point-to-point (design time)**

Area Usage

- **Point-to-point (direct connection)**
- **Multi-Layer NoC**
- **Packet+Circuit Switched NoC**

Reduce long wires problem

- **Point-to-point (no)**
- **Multi-Layer NoC (yes)**
- **Standard NoC (yes)**
Each control router can control the configuration of the data routers in the same XY coordinates.