

# Breaking Elliptic Curves Cryptosystems using Reconfigurable Hardware

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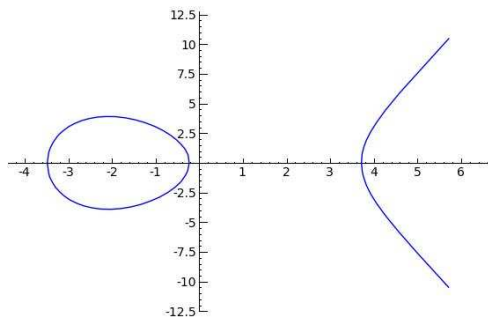
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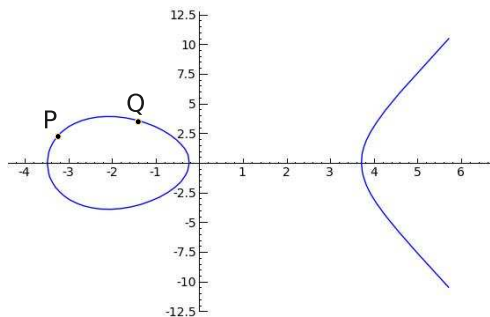
◁ Radboud University Nijmegen, Netherlands

August 31, 2010

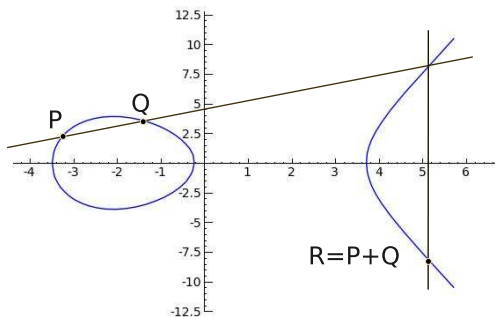
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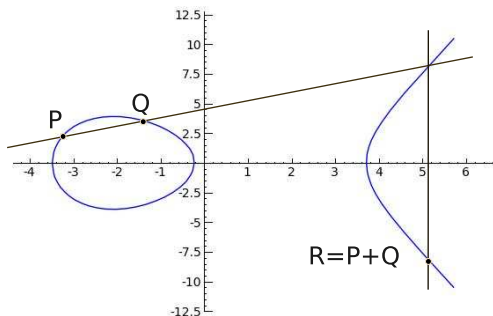


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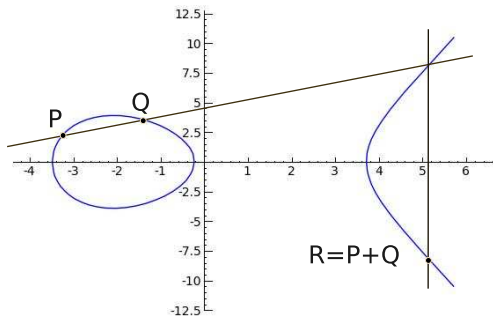
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$$Q \leftarrow [k]P$$

$$= P + P + \dots + P.$$



# Elliptic Curve Cryptography



Point Multiplication:

$$Q \leftarrow [k]P \\ = P + P + \dots + P.$$

Elliptic Curve Discrete  
Logarithm Problem  
(ECDLP):

Given  $Q$  and  $P$ , find  $k$   
such that  
 $Q = [k]P$ .

# Certicom challenge

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- Lunched by Certicom in 1997



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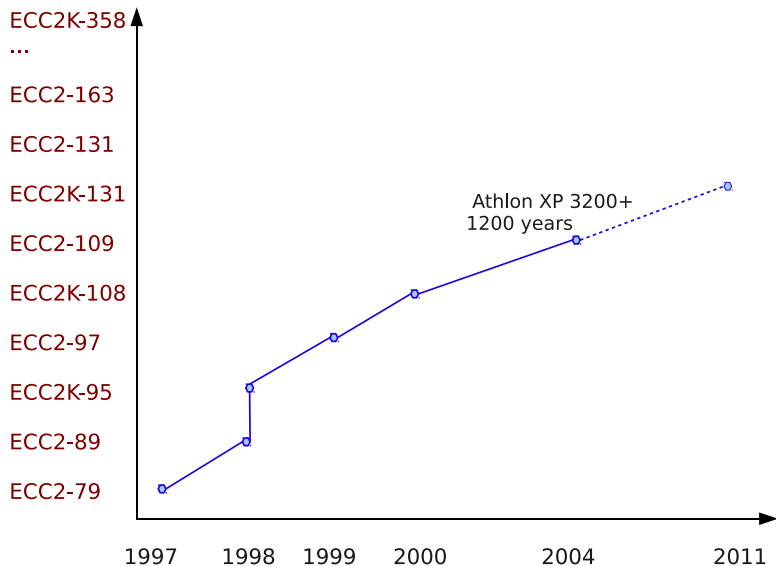
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ECC on $GF(2^m)$	ECC on $GF(p)$
ECC2-79	ECCp-79
ECC2-89	ECCp-89
ECC2K-95	ECCp-97
ECC2-97	ECCp-109
ECC2K-108	ECCp-131
ECC2-109	ECCp-163
ECC2K-130	ECCp-191
ECC2-131	ECCp-239
ECC2-163	ECCp-359
...	
ECC2K-358	

# Certicom challenge



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- **The challenge** : find  $k$  such that  $Q = [k]P$ .

# The Ev11 Project

- Target : solve ECC2K-130
- Methods: Parallelized Pollard rho
- Platforms:
  - General Purpose CPU (Compute clusters)
  - Graphics card clusters
  - Playstation clusters
  - FPGA clusters
  - ASICs (Estimation)
- Status:
  - Globally distributed (Netherlands, Belgium, Ireland, USA, Taiwan, Switzerland, ..)
  - Progress report: <http://www.ecc-challenge.info/>



# Parallelized Pollard rho

## Pollard rho

finding  $(c_i, d_i)$  and  $(c_j, d_j)$  such that

$$[c_i]P + [d_i]Q = [c_j]P + [d_j]Q$$

$$[(c_i - c_j)]P = [(d_j - d_i)]Q$$

since  $Q \equiv [k]P$ ,

$$k \equiv (c_i - c_j)(d_j - d_i)^{-1} \pmod{n}.$$

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## Random walk

- Start with  $R_0 = [c_0]P + [d_0]Q$
- Iteration function  
 $\{c_{i+1}, d_{i+1}, R_{i+1}\} \leftarrow f(c_i, d_i, R_i)$   
such that  $R_i = [c_i]P + [d_i]Q$

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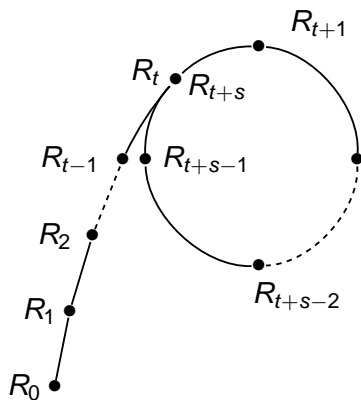
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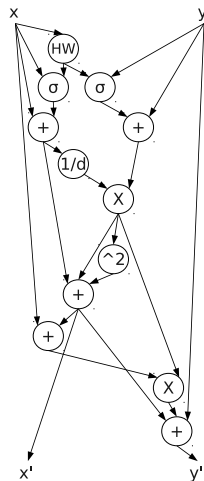
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$$j = ((HW(x)/2) \bmod 8) + 3$$

$$\sigma^j(x), \sigma^j(y)$$

$$dx = x + \sigma^j(x)$$

$$dy = y + \sigma^j(y)$$

$$s = 1/dx$$

$$\lambda = s * dy$$

$$\lambda^2$$

$$x' = dx + \lambda + \lambda^2$$

$$x' + x$$

$$(x' + x) * \lambda$$

$$y' = y + x' + (x' + x) * \lambda$$

# FPGA platform : COPACOBANA-3



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- Xilinx Spartan-3 FPGA (XC3S5000)
- 128 FPGA units in total (16 x 8)
- 33,280 slices and 104 BRAMs available on one FPGA

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 $\mathbf{P} = \{ 1, w, w^2, \dots, w^{130} \}.$
  - Type II normal basis:  
 $\mathbf{N} = \{ \gamma + \gamma^{-1}, \gamma^2 + \gamma^{-2}, \gamma^{2^2} + \gamma^{-2^2}, \dots, \gamma^{2^{130}} + \gamma^{-2^{130}} \}.$

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- Architecture
  - digit-serial
  - pipe-lined

# Shokrollahi's multiplication algorithm

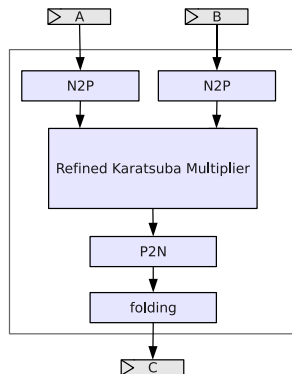
Fast conversion between

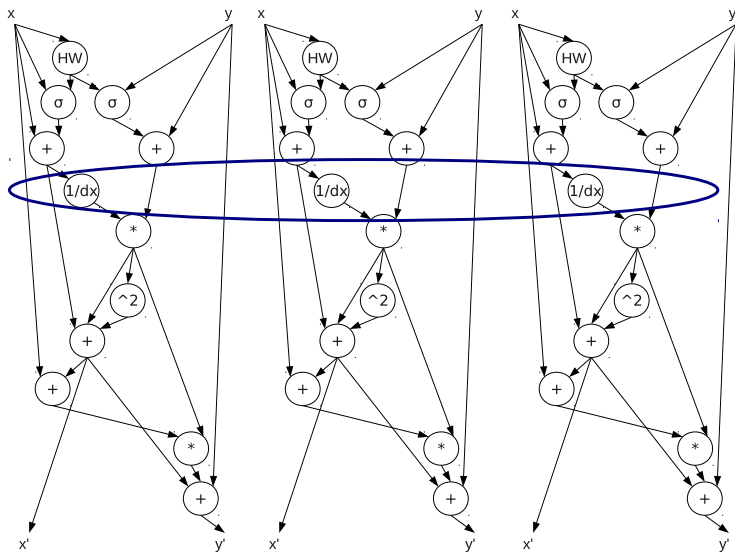
- permuted Normal **pN** basis

$$\{\gamma + \gamma^{-1}, \gamma^2 + \gamma^{-2}, \gamma^3 + \gamma^{-3}, \dots, \gamma^{131} + \gamma^{-131}\}.$$

- new Polynomial **nP** basis

$$\{(\gamma + \gamma^{-1}), (\gamma + \gamma^{-1})^2, \dots, (\gamma + \gamma^{-1})^{131}\}.$$





# Batch Inversion

Montgomery's trick for batch inversion (Batch size = 3)

**Input:**  $\alpha_1, \alpha_2, \alpha_3$ .

**Output:**  $\alpha_1^{-1}, \alpha_2^{-1}$  and  $\alpha_3^{-1}$ .

1:  $d_1 \leftarrow \alpha_1$

2:  $d_2 \leftarrow d_1 \alpha_2$

3:  $d_3 \leftarrow d_2 \alpha_3$

4:  $u \leftarrow d_3^{-1}$

5:  $t_3 \leftarrow u d_2, u \leftarrow u \alpha_3$

6:  $t_2 \leftarrow u d_1, u \leftarrow u \alpha_2$

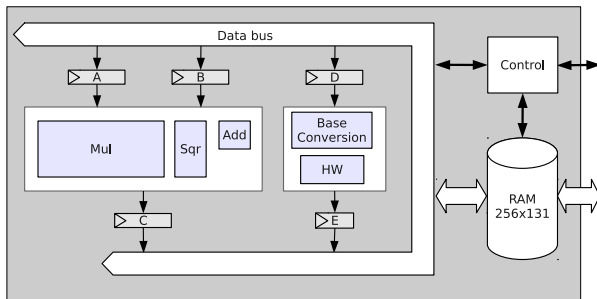
7:  $t_1 \leftarrow u$

**Return:**  $t_1, t_2, t_3$ .

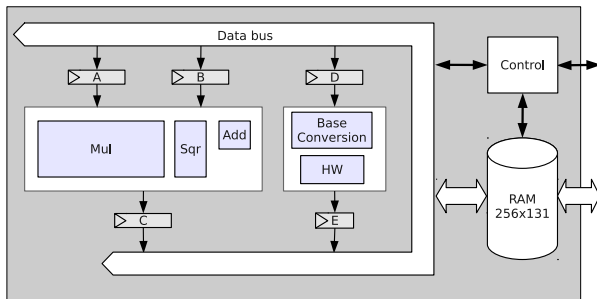
- we trade **I** for **3M + I/n**.
- One iteration: **2M + 3M + I/n**.

Polynomial basis representation, digit-serial multiplier, load/store architecture.

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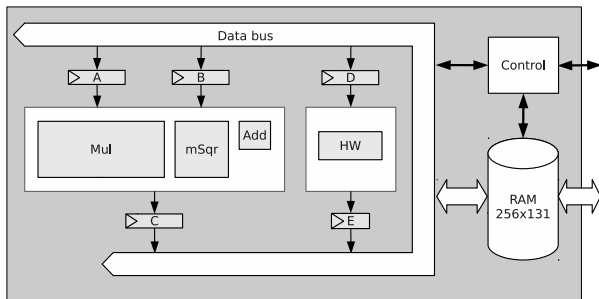


- Area : 3656 slices (Multiplier: 1468; conversion :1206)
- Frequency : 101 MHz
- 71 cycles per iteration

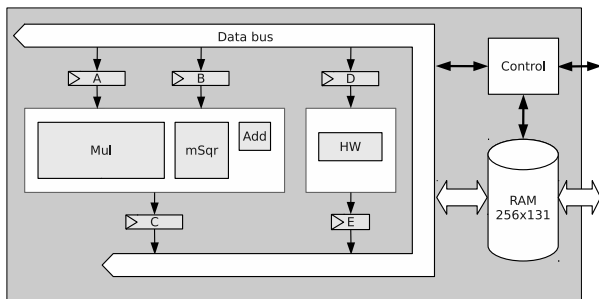
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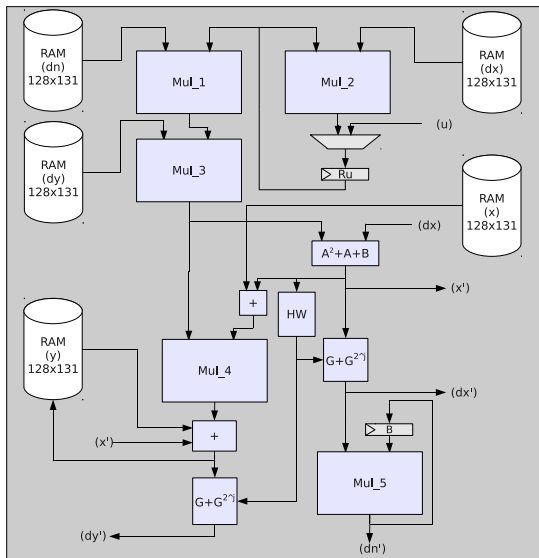
## Normal basis representation, digit-serial multiplier (Kwon), load/store architecture



- Area : 2578 slices (Multiplier: 2093)
- Frequency : 125 MHz
- 81 cycles per iteration

# Normal basis representation, Shorollahi multiplier (pipe-lined), Fully pipe-lined architecture

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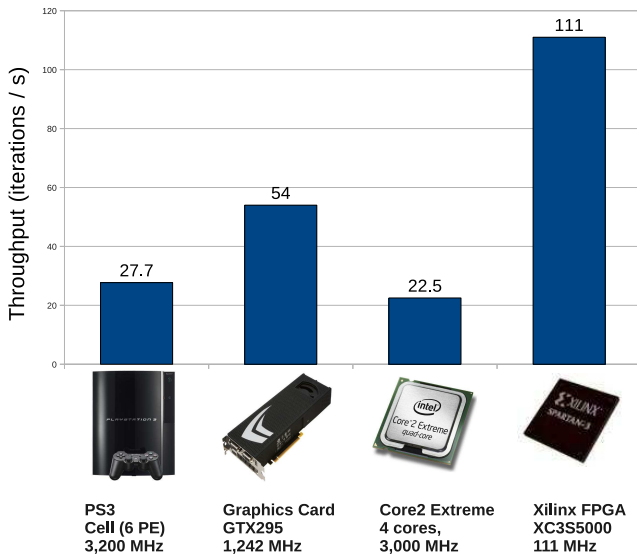


## Performance of Archi-I, Archi-II and Archi-III

	Area	Freq.	Delay	Clones	Throughput per FPGA
	#slice /#BRAM	[MHz]	[Cycles]		
<i>Archi-I:</i> Polynomial	3,656 / 4	101	71	9	$12.8 \times 10^6$
<i>Archi-II:</i> Type-II ONB	2,578 / 4	125	81	12	$18.5 \times 10^6$
<i>Archi-III:</i> Shokrollahi's	26,731 / 20	111	23 *	1	$111 \times 10^6$

\* The average throughput is one iteration per cycle.

# Comparison with CPU, Play station 3 and GPU



# Effort estimation

- One FPGA finishes  $111 \times 2^{20}$  iterations per second

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- One COPACOBANA-3 includes 128 FPGAs  
 $\Rightarrow 128 \times 111 \times 2^{20} \times 3600 \times 24 \times 365 = 2^{58.7}$  per year



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⇒  $128 \times 111 \times 2^{20} \times 3600 \times 24 \times 365 = 2^{58.7}$  per year
- $2^{60.9}$  iterations are expected  
⇒ Given 5 COPACOBANA-3 clusters, we can solve the ECC2K-130 in one year!

# Conclusion

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- Low-cost FPGA show good performance/cost ratio compared with CPU, Play Station 3 and GPU.
- ECC2K-130 is practically solvable.



D. V. Bailey, L. Batina, D. J. Bernstein, P. Birkner, J. W. Bos, H. Chen, C. Cheng, G. van Damme, G. de Meulenaer, L. J. D. Perez, J. Fan, T. Güneysu, F. Gurkaynak, T. Kleinjung, T. Lange, N. Mentens, R. Niederhagen, C. Paar, F. Regazzoni, P. Schwabe, L. Uhsadel, A. Van Herrewege, and B. Yang.

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